

Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application:

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Claim 1 (original): A method for communicating between computer bus modules comprising the steps of:

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converting native bus signals from a first computer module to a first point-to-point interface;

conveying the bus signals using the first point-to-point interface to a bus emulator;

conveying the bus signals from the bus emulator using a second point-to-point interface to a second computer module; and

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converting the bus signals received at the second computer to a native form.

Claim 2 (currently amended): The method of Claim 1 wherein the step of converting native bus signals from a first computer module to a first point-to-point interface comprises the steps of:

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monitoring the native bus signals in order to identify the beginning of a data transfer cycle; and

accepting data and address signals from the native bus and serializing these together with an indication of the a type of for the data transfer cycle identified.

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Claim 3 (original): The method of Claim 1 wherein the step of conveying bus signals from the bus emulator to a second computer module comprises the steps of:

receiving the bus signals from the first point-to-point interface in the bus emulator;

translating the first point-to-point interface received in the bus emulator to a bus structure internal to the bus emulator;

5 conveying the bus signals received in the bus emulator by way of the first point-to-point interface onto said bus structure; and

translating the bus signals carried on said bus structure to a second point-to-point interface.

10 Claim 4 (original): The method of Claim 3 wherein the step of conveying the bus signals received in the bus emulator by way of the first point-to-point interface onto said bus structure comprises the steps of:

granting said bus structure to the first point-to-point interface if said bus structure is available; and

15 propagating the bus signals translated from the first point-to-point interface onto the bus structure if the bus structure is granted to said first point-to-point interface.

Claim 5 (original): A computer system comprising:

20 plurality of point-to-point interface units comprising a computer module interface and a point-to-point interface;

plurality of computer modules connected to the computer module interface of the plurality of point-to-point interface units; and

25 bus emulator connected to the point-to-point interface of the plurality of point-to-point interface units.

Claim 6 (original): The computer system of Claim 5 wherein the plurality of point-to-point interface units comprise parallel-to-serial conversion units that operate upon detecting the beginning of a data transfer cycle presented to the
30 computer module interface and wherein the parallel-to-serial conversion units

accept a data field and an address field and a cycle-type indicator from the computer module interface.

5 Claim 7 (original): The computer system of Claim 5 wherein the plurality of point-to-point interface units comprise high-current parallel drivers capable of propagating data, address and data transfer cycle requests.

10 Claim 8 (original): The computer system of Claim 5 wherein the bus emulator comprises:
plurality of point-to-point interfaces interconnected by an internal bus.

15 Claim 9 (original): The computer system of Claim 8 further comprising an arbiter for granting access to the internal bus to one of the plurality of point-to-point interfaces.

Claim 10 (currently amended): The computer system of Claim 8 further comprising a cascade port that connects to the internal bus and can be used to extend ~~the~~ a length of the internal bus.

20 Claim 11 (original): A computer module comprising a point-to-point interface.

Claim 12 (original): The computer module of Claim 11 wherein the point-to-point interface comprises:

25 parallel-to-serial conversion unit that operate upon detecting the beginning of a data transfer cycle presented to the computer module interface and wherein the parallel-to-serial conversion units accept a data field and an address field and a cycle-type indicator from the computer module interface and delivers a serial output comprising a data transfer cycle to the point-to-point interface.

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Claim 13 (original): The computer module of Claim 11 wherein the point-to-point interface comprises high-current parallel drivers capable of propagating data, address and data transfer cycle requests.

- 5 Claim 14 (original): A point-to-point interface unit comprising a computer module interface and a point-to-point interface.

Claim 15 (original): The point-to-point interface unit of Claim 14 further comprising parallel-to-serial conversion unit that operate upon detecting the
10 beginning of a data transfer cycle presented to the computer module interface and wherein the parallel-to-serial conversion units accept a data field and an address field and a cycle-type indicator from the computer module interface and delivers a serial output comprising a data transfer cycle to the point-to-point interface.

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Claim 16 (original): The computer system of Claim 14 wherein the plurality of point-to-point interface units comprise high-current parallel drivers capable of propagating data, address and data transfer cycle requests.

- 20 Claim 17 (original): A bus emulator comprising:
internal bus; and
plurality of point-to-point interfaces interconnected by the internal bus.

Claim 18 (original): The bus emulator of Claim 17 an arbiter for granting
25 access to the internal bus to one of the plurality of point-to-point interfaces.

Claim 19 (currently amended): The bus emulator of Claim 17 further comprising a cascade port connected to the internal bus and can be used to extend ~~the~~ a length of the internal bus.